VLSI Education: FPGA - ASIC Pipeline and Toolchain

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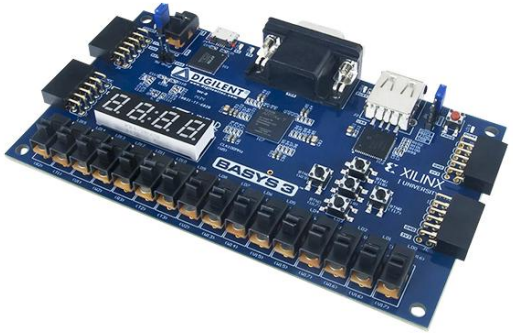
Outline

Introduction

- ASIC Education is generally speaking sparce at the Undergraduate Level
- In the past we've done some ASIC design with Undergrads using industry standard tools [1]
- I want students to start going from the FPGA course and start designing their own Integrated Circuits.
- This means creating a clean path from FPGA course work to Practical ASIC Design

Digital Systems Design

- Design, implementation and testing of a digital system. Mask programmable and field programmable technology. Logic design for integrated systems. Design for testability. Real versus ideal logic design. CAD tools for digital systems design: simulation, synthesis and fabrication.



Project Marking

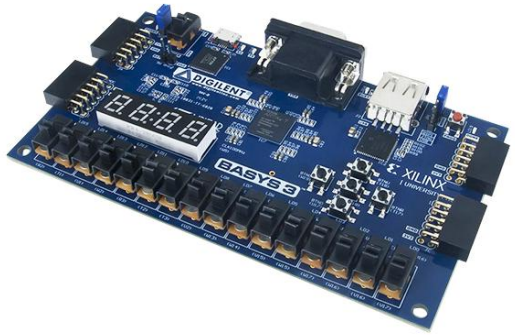
- We change the marking structure depending on how the lab difficulty is distributed.
- The percentage that each lab is worth varies from below 1% to 30%.
- This means that more time can be spent on labs which actually test understanding.

Component	**Weight 2023**
Lab 1 Code/Documentation/Video	1%
Lab 2 Code/Documentation/Video	2%
Lab 3 Code/Documentation/Video	2%
Lab 4 Code/Documentation/Video	10%
Lab 4 Demo/Design/Code/Oral Exam	15%
Midterm Exam	20%
Final Exam	50%

Table: Course assessment weighting (2023).

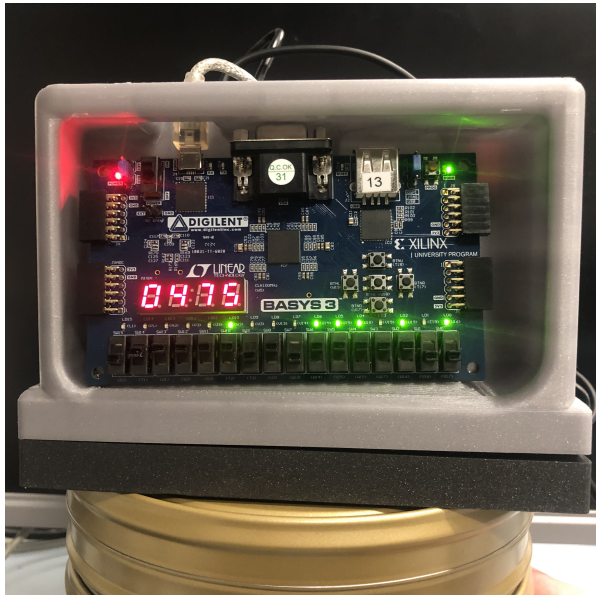
Having Enough FPGAs

- Ideally we would want each student to take one heavily featured FPGA home.
- Good FPGA boards are expensive. The basys3 board is $235.00 CAD off Newark.
- We've had various plays on sharing FPGAs between students.



4 FPGAs to a Dozen Students

- As mentioned, FPGAs are expensive.
- But we'd like students to have continual access.
- Based on simplifying earlier work for remote access to FPGAs



Apple Silicon

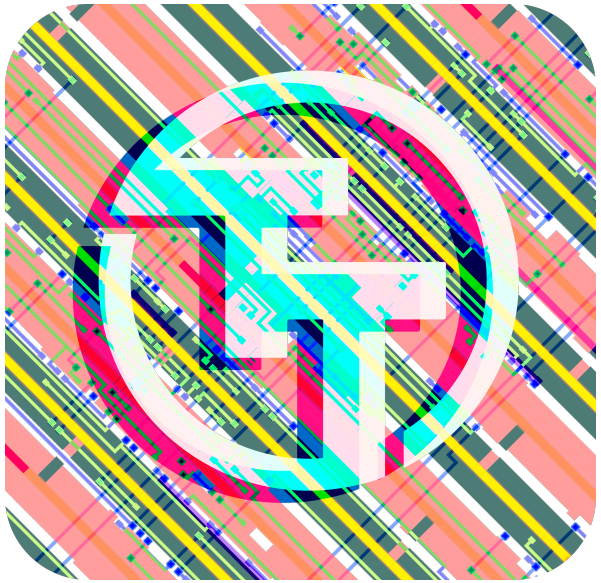
- I would like it if all students had a standardized Linux Laptop
- **I will not be getting my way!**
- Windows VMs are no Longer a good solution.
- So I’ve put together instructions for running the open source toolchain via an ARC Mac.
- These are publicly available on I’ll have a link at the end.

Public Labs

- To help others make use of this work the 2023 Lab set are publicly available for anyone to make use of.
- This includes scripts for compiling answer bitstreams, clarifications from that run, and full tex files.
- The full lab set is avaialble at: https://github.com/devinatkin/ENEL453-Labs
- One of the labs from this set is also included in: https://github.com/devinatkin/tt05-stopwatch

Tiny Tapeout

- Tiny Tapeout offers a cheaper open alternative to the closed source paths [2]
- Tiny Tapeout Large class package can do: Up to 75 Projects, 5 PCB kits, From, €5325



MicroTiles

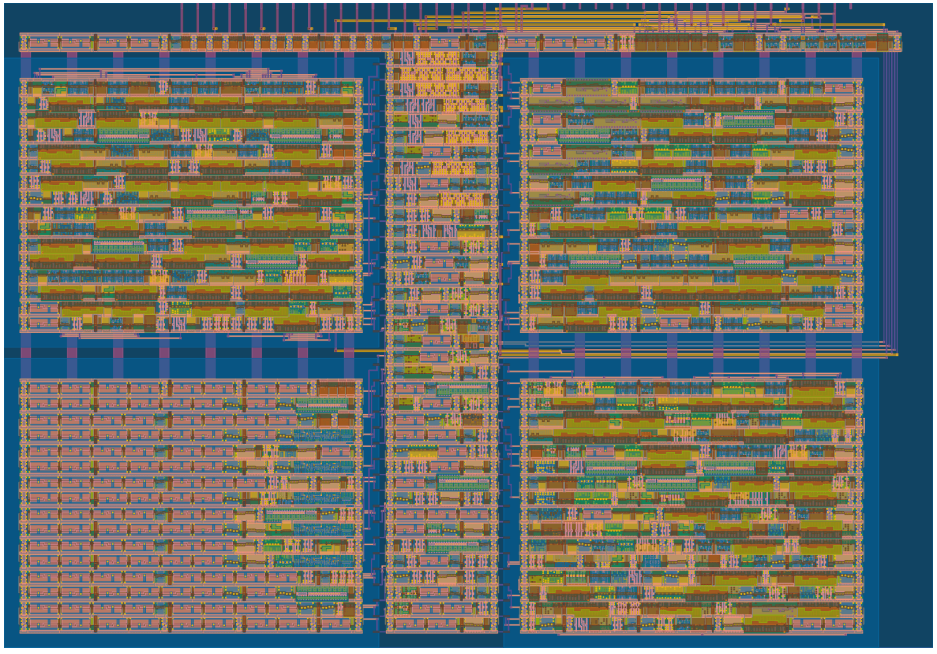


Figure: Microtiles - 4 Projects on 1 Tile

If €5325 and 75 Projects is not enough. Then using microtiles increases that up to 300 projects.

TT05 Example Project

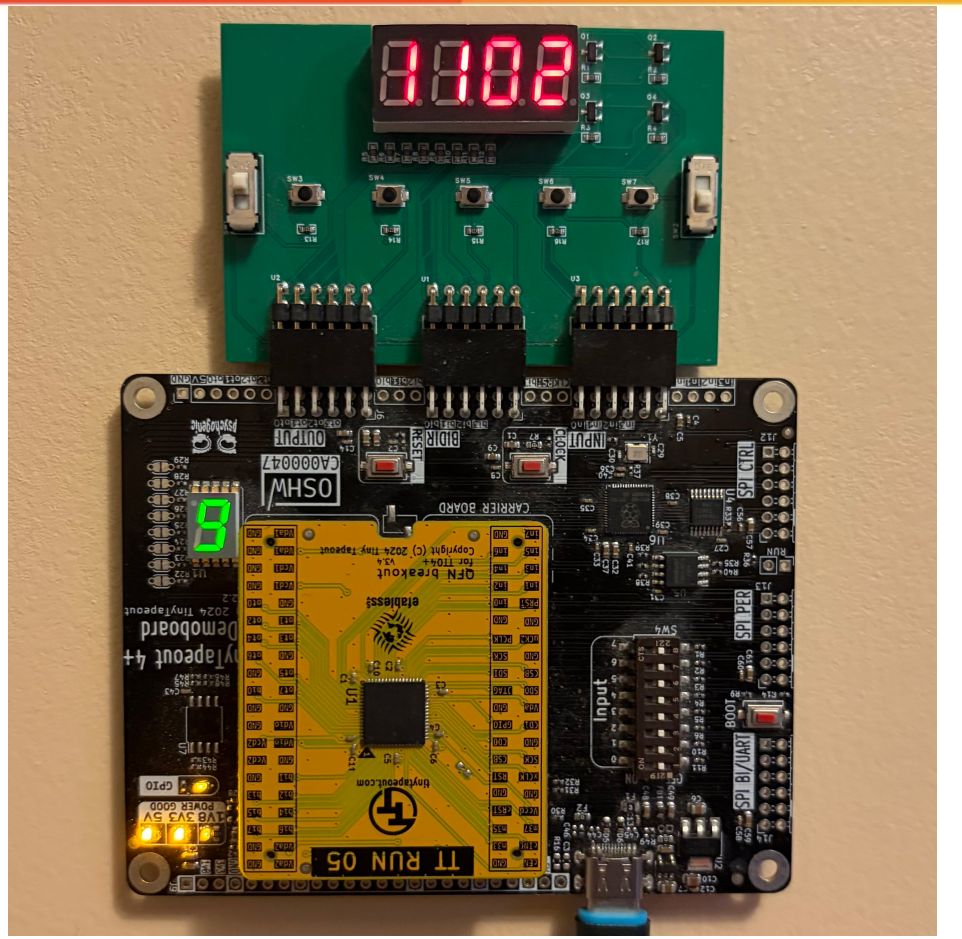


Figure: ENEL 453 Lab on Silicon

The Lab 3 from the ENEL 453 2023 Lab set is reproduced in this TT05 Project.

Conclusions

- I still need to get a lot of in-situ feedback on this content. Although early comments have been generally positive.
- Additional Lab sets would be good to transition to ASIC output and to expand the available public labs
- Mac OS is going to continue to grow. The git first approach using github actions may solve the problem if a course is heavily git centered
- Web Access is somewhat solved with a large enough board set. But for many it’s an ongoing issue.

Pi Bitstream Github

Figure: Bitme Repository

ENEL 453 Labs

Figure: ENEL 453 Lab Repository

Apple Silicon FPGA Development

Figure: Mac FPGA Setup Page

References I

[1] D. Atkin and O. Yadid-Pecht, "A case study in vlsi education during the covid-19 pandemic," in Proceedings of the Canadian Engineering Education Association (CEEA), CEEA-ACÃG23, Paper 129, Okanagan College and UBC-Okanagan, June 18–21, 2023, 2024. DOI: 10.24908/pceea.2023.17137. [Online]. Available: https://doi.org/10.24908/pceea.2023.17137.

[2] M. D. Venn, "Tiny tapeout: A shared silicon tapeout platform accessible to everyone," TechRxiv, Jul. 2024, Preprint. DOI: 10.36227/techrxiv.172055642.27780676/v1.

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